Quad LVDS Line Driver

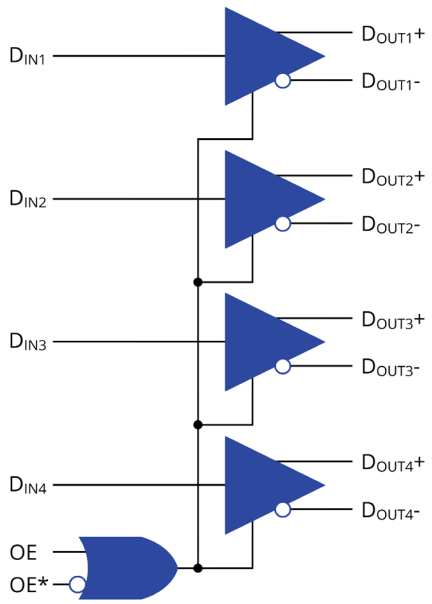
Features

- DC to 400 Mbps / 200 MHz low noise, low skew, low power operation
  - 300 ps (max) channel-to-channel skew
  - 250 ps (max) pulse skew
  - 23 mA (max) power supply current
- LVDS outputs conform to TIA/EIA-644-A standard
- Standard output enable scheme eliminates power consumption when device is not in use
- Latch-up immune due to dielectric isolation
- Available in space saving SOIC-16 package
- Extended temperature range: -40 °C to +85 °C

Applications

- Data Communications
- Satellite Systems
- Launch Vehicles

Function Diagram



Description

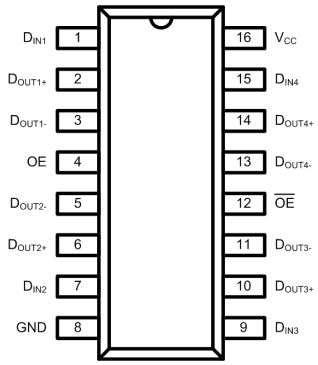
The LVDS031 is a 400 Mbps Quad LVDS (low voltage differential signaling) Line Driver optimized for high-speed, low power, low noise transmission over controlled impedance (approximately 100Ω) transmission media (e.g. cables, printed circuit board traces, backplanes).

The LVDS031 accepts four LVCMOS / LVTTL signals and translates them to four LVDS signals. Its differential outputs can be disabled and put in a high-impedance state via two enable pins, OE and OE*.

Low 300 ps (max) channel-channel skew and 250 ps (max) pulse skew ensure reliable communication in high-speed links that are highly sensitive to timing error.

Supply current is 23 mA (max). LVDS outputs conform to the ANSI/EIA/TIA-644-A standard. The LVDS031 is offered in 16-pin SOIC package and operates over an extended -40 °C to +85 °C temperature range.

Pin Diagram



Logic Table

OE	OE*	D_{OUT+}	D_{OUT-}
0	0	Enabled	Enabled
0	1	Disabled	Disabled
1	0	Enabled	Enabled
1	1	Enabled	Enabled

Pin Descriptions

PIN NAME	PIN NUMBER	PIN DESCRIPTION
D_{IN1}, D_{IN2}, D_{IN3}, D_{IN4}	1, 7, 9, 15	Driver LVCMOS input pins.
D_{OUT1+}, D_{OUT1-}, D_{OUT2+}, D_{OUT2-}, D_{OUT3+}, D_{OUT3-}, D_{OUT4+}, D_{OUT4-},	2, 3, 5, 6, 10, 11, 13, 14	Non-inverting and inverting LVDS output pins.
OE, OE*	4, 12	Driver output enable pins. When OE is high or OE* is low or open, the driver outputs are enabled. When OE is low and OE* is high, the driver outputs are disabled.
V_{CC}	16	Power supply pin. Bypass V_{CC} to GND with 0.1 µF and 0.01 µF ceramic capacitors.
GND	8	Ground or circuit common pin.

Absolute Maximum Ratings *(NOTE1)*

V_{CC} to GND ..... -0.3 V to +4 V

Inputs
OE, OE*, D_{IN} to GND ..... -0.3 V to V_{CC} +0.3 V

Outputs
D_{OUT+}, D_{OUT-} to GND ..... -0.3 V to V_{CC} +0.3 V

SOIC-16 Thermal Resistance
Θ_{JC} ..... 44 K/W
Θ_{JA} ..... 81 K/W

T_{stg} - Storage temperature range ..... -65 °C to +150 °C
T_J - Junction operating temperature ..... +150 °C
T_L - Lead temperature (soldering, 1s) ..... +260 °C

ESD Ratings
HBM *(NOTE2)* ..... 8 kV
MM *(NOTE2)* ..... 250 V
CDM *(NOTE2)* ..... 1.25 kV

NOTE1 *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTE2
HBM - Human Body Model, applicable standard JESD22-A114-C
MM - Machine Model, applicable standard JESD22-A 115-A
CDM - Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

Symbol	Parameter	Pins	MIN	TYP	MAX	Unit
V_{CC}	Supply voltage	V_{CC}	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	OE, OE*, D_{IN}	2.0		V_{CC}	V
V_{IL}	Low-level input voltage	OE, OE*, D_{IN}	0		0.8	V
T_A	Operating free-air temperature range		-40	25	85	°C

Electrical Characteristics

Over recommended operating conditions ***(NOTE3)***, T_A = 25 °C, V_{CC} = 3.3 V, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
LVCMOS Input Specifications (OE, OE*, D_{IN} pins)						
V_{IH}	High-level input voltage		2.0		V_{CC}	V
V_{IL}	Low-level input voltage		GND		0.8	V
I_{IH}	High-level input current	V_{CC} = 3.6 V V_{IN} = 3.6 V	-10		10	µA
I_{IL}	Low-level input current	V_{CC} = 3.6 V V_{IN} = 0 V	-10		10	µA
V_{CL}	Input clamp voltage ***(NOTE4)***	I_{CL} = -18 mA, V_{CC} = 0 V	-1.5	-0.9		V

Electrical Characteristics *(CONTINUED)*

Over recommended operating conditions ***(NOTE3)***, T_A = 25 °C, V_{CC} = 3.3 V, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
LVDS Output Specifications (D_{OUT+}, D_{OUT-} pins)						
$\|V_{OD}\|$	Differential output voltage magnitude	R_L = 100 Ω Figure 1	250	370	450	mV
$\|\Delta V_{OD}\|$	Change in magnitude of V_{OD} for complimentary output states		-35		35	mV
$V_{OCM(ss)}$	Steady-state output common mode voltage		1.125	1.25	1.375	mV
$\Delta V_{OCM(SS)}$	Change in magnitude of $V_{OCM(ss)}$ for complementary output states		-25		25	mV
V_{OH}	Output high voltage	R_L = 100 Ω Figure 1		1.43	1.6	V
V_{OL}	Output low voltage		0.9	1.06		V
I_{OS}	Output short circuit current ***(NOTE5)***	Enabled, D_{OUT+} or D_{OUT-} = 0 V			-13	mA
I_{OSD}	Differential output short circuit current ***(NOTE5)***	Enabled, V_{OD} = 0 V			-13	mA
I_{OZ}	High-impedance output current	Disabled, V_{OUT} = 0 V or V_{CC}	-14		14	µA
C_{OUT}	Output capacitance	D_{OUT+} or D_{OUT-} to GND		3		pF
Power Supply Current Specifications						
I_{CC}	Power supply current without output loads	Enabled, D_{IN} = 0 V or V_{CC}		1	2	mA
I_{CCL}	Power supply current with output loads	Enabled, D_{IN} = 0 V or V_{CC}, R_L = 100 Ω		16	23	mA
I_{CCZ}	Power supply current with disabled outputs	Disabled, OE = 0 and OE* = 1		1	2	mA

NOTE3 *Current into device pin is defined as positive. Current out of the device is defined as negative. All voltages are referenced to ground, unless otherwise specified.*

NOTE4 *This specification is not production tested and is guaranteed by design simuiations.*

NOTE5 *Output short circuit current (I_{0S}) is spedfied as magnitude only. The minus sign indicates direction only.*

Switching Characteristics

Over recommended operating conditions ***(NOTE3)***, T_A = 25 °C, V_{CC} = 3.3 V, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
LVDS AC Specifications ***(NOTES 6, 7, 8)***						
t_{PLH}	Propagation delay, low-to-high	R_L = 100 Ω C_L = 15 pF ***(NOTE14)*** Figures 2 and 3	0.6	1	1.9	ns
t_{PHL}	Propagation delay, high-to-low		0.6	1.5	2	ns
t_r	Rise time		0.5	0.7	1	ns
t_f	Fall time		0.5	0.7	1	ns
$t_{SK(p)}$	Pulse skew ***(NOTE9)***			50	250	ps
$t_{SK(c-c)}$	Channel-to-channel skew ***(NOTE10)***			50	300	ps
$t_{SK(p-p)A}$	Part-to-part skew ***(NOTE11)***				1	ns
$t_{SK(p-p)B}$	Part-to-part skew ***(NOTE12)***				1.3	ns
t_{PLZ}	Disable time, low-to-high Z	R_L = 100 Ω C_L = 15 pF ***(NOTE14)*** Figures 4 and 5			5	ns
t_{PHZ}	Disable time, high-to-high Z				5	ns
t_{PZL}	Enable time, high Z-to-low				5	ns
t_{PZH}	Enable time, high Z-to-high				5	ns
f_{MAX}	Maximum operating frequency ***(NOTE13)***	Figure 2	200	250		MHz

NOTE6 *Generator output characteristics (unless otherwise specfied): f = 1 MHz, Z_0 = 50 Ω, t_r < 1 ns, t_f < 1 ns*

NOTE7 *All Input voltages are for one channel unless otherwise specified. Other inputs are set to GND.*

NOTE8 *Switching Characteristic specification are not production tested and are guaranteed by statistical analysis of characterization data.*

NOTE9 *$t_{SK(p)}$, pulse skew, is the magnitude difference in propagation delay time between the positive going edge and the negative going edge of the same channel ($t_{SK(p)} = |t_{PLH} - t_{PHL}|$).*

NOTE10 *$t_{SK(c-c)}$, channel-to-channel skew, is the difference in propagation delay time between channels on the same device at any operating temperature and supply voltage.*

NOTE11 *$t_{SK(p-p)A}$, part-to-part skew "A", is the difference in propagation delay time between devices operating at the same power supply voltage and within 5 °C of each other within the operating temperature range.*

NOTE12 *$t_{SK(p-p)B}$, part-to-part skew "B", is the difference in propagation delay time between devices operating at any recommended power supply voltage and ambient temperature. It is also defined as |MIN -MAX| propagation delay (t_{PLH} or t_{PHL}).*

NOTE13 *Generator output characteristics for the f_{MAX}: Z_0 = 50 Ω, $t_r = t_f$ < 1 ns, 50 % duty cycle, 0 V to 3 V amplitude. Output criteria for f_{MAX}: 45 % / 55 % duty cycle, V_{OD} ≥ 250 mV.*

NOTE14 *The capacitive load C_L includes test fixture, probe and lumped capacitance.*

Test Circuits and Timing Diagrams

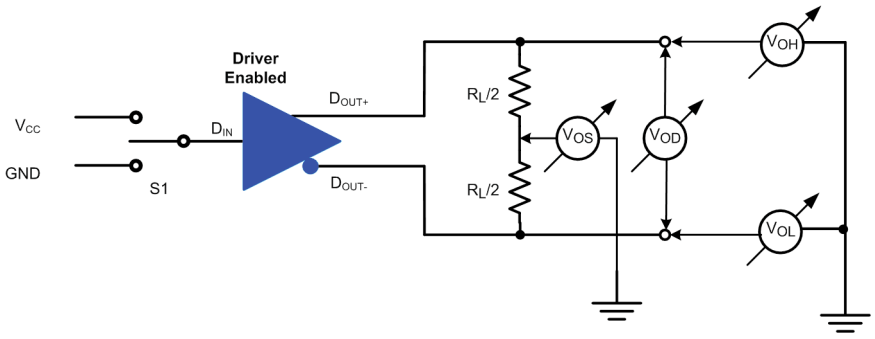


Figure 1. Driver V_{OH} and V_{OL} Test Setup

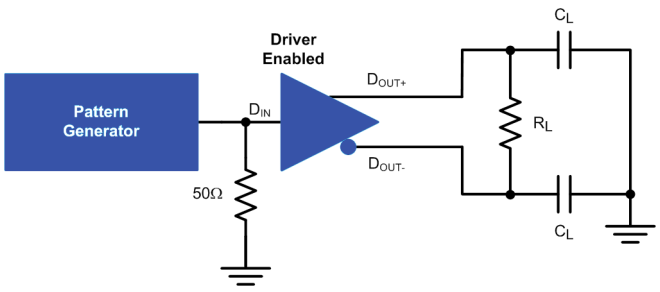


Figure 2. Driver Propagation Delay and Transition Time Test Setup

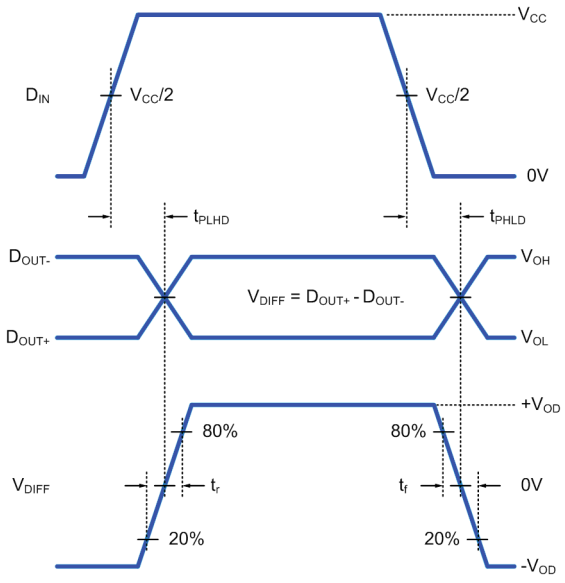


Figure 3. Driver Propagation Delay and Transition Time Waveforms

Test Circuits and Timing Diagrams

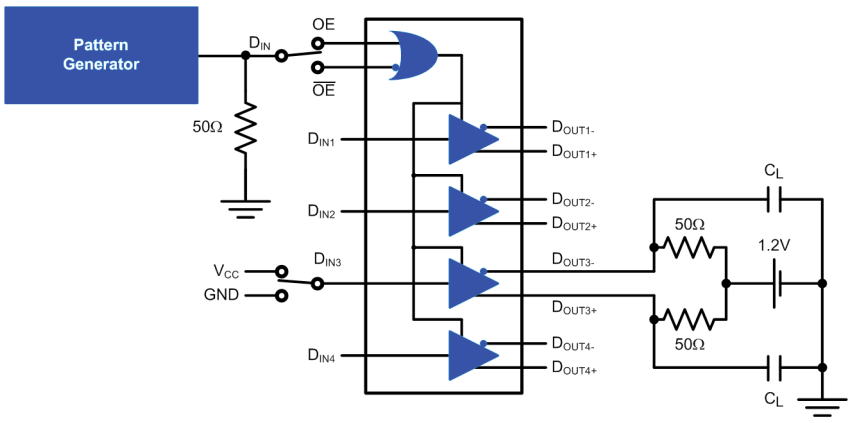


Figure 4. Driver High-Z Delay Test Setup

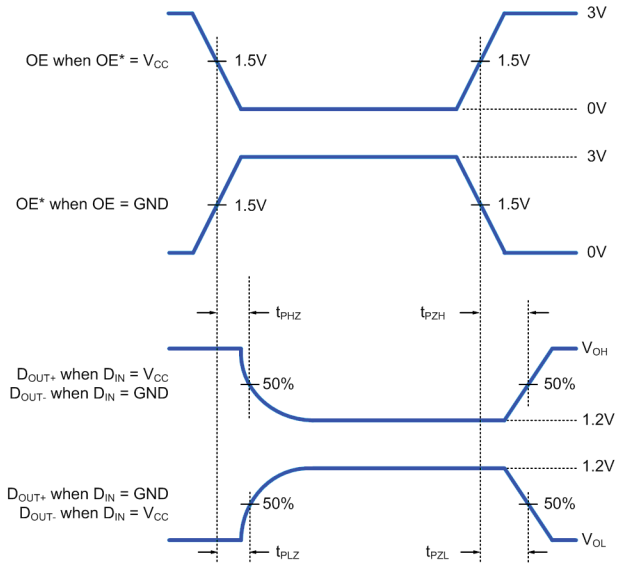


Figure 5. Driver High-Z Delay Waveforms

Application Information

ABOUT LVDS

Due to bandwidth and power consumption, high speed communication links usually use differential signaling. In this area LVDS provides an outstanding performance to power ratio: It offers a high bandwidth at very low power consumption and low EMI. Therefore it is used extensively for audio and video transmission, ASIC and FPGA I/O, sensor data transmission, clock distribution and a lot more signaling tasks.

COMMON MODE

Large switching currents in an electrical system may result in a momentary voltage drop in supply voltage and/or in a local raise of the ground potential. In terms of the instantaneous ground potential shift this behaviour is known as ground bounce.

This reaction to high currents may be reduced by proper design and size of ground and supply planes and the use of low resistive decoupling capacitors, but they cannot be eliminated totally.

Another effect in this context is a steady-state potential difference between ground connections: Each connection generates a voltage drop which follows Ohm's Law (U = R * I). As a result the ground potential difference between a module and the main ground plane rises linearly with current and terminal resistance. Since the terminal resistance may increase by aging, the ground potential of the connected module may drift more and more resulting in a higher steady-state potential difference.

In both situations, ground bounce and ground drift, the common mode difference between transmitter and receiver may exceed the specified +/- 1 Volt defined by the LVDS standard resulting in communication errors or even link interruption. These effects have already been reported in Avionics, Industrial applications, by telecommunication companies and automobile manufacturers.

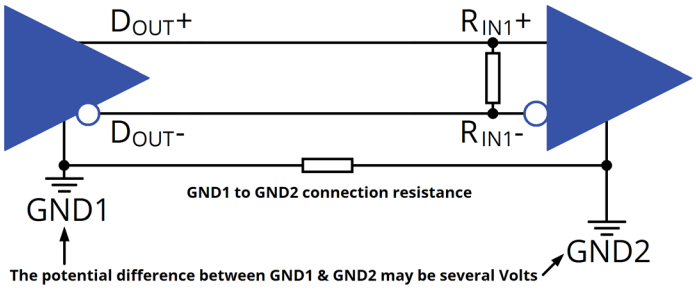


Figure 6. GND-potential difference

POSSIBLE SOLUTION: AC COUPLING?

One possibility to eliminate common mode differences caused by ground potential issues is the use of coupling capacitors on both channels of the differential pair. But there is a big constraint: Capacitive coupling is only convenient for DC balanced data. This means that the data has to have an equal number of ones and zeros. But generally this is not the case for non-coded data, audio, video, sensor or control signals. And if the data would be coded in order to get a balanced signal, this would have an impact on the bandwidth. In case of 8b/10b coding the net data rate will decrease by 20 %.

RS-485

In noisy environments and applications with known common mode issues usually the RS-485/422 is used due to its large swing differential standard which guarantees communication at common modes of -7 to +12 Volts. Its disadvantages are the low data rate and the poor bandwidth to power and EMI performance.

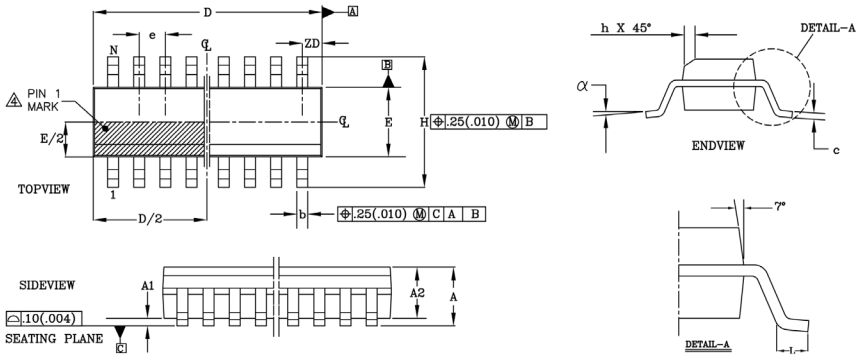
EXTENDED COMMON-MODE LVDS: COMBINING THE ADVANTAGES

Having a look at the LVDS standard, the noise margin may be sufficient on single PCBs or in small boxed systems. But in noisy environments or larger distributed systems or box-to-box communication, the small +/-1 V common mode window potentially leads to communication problems, particularly over the lifetime of the system.

RS-485 offers a much better noise margin but shows very poor performance regarding power consumption, speed and EMI.

Extended common-mode LVDS combines the benefits of LVDS and RS-485: It's fully compatible with the LVDS standard in terms of signal levels, speed, power and EMI, showing the standard pinout and footprint. The extended common mode of -7 to +12 Volt finally makes it a perfect choice for harsh environments. Also it works as a high-performance replacement for RS-485 applications.

Package Dimensions (SOIC-16)



SYMBOL	SOIC-16LD MILLIMETERS	
	MIN	MAX
A1	0.10	0.25
B	0.36	0.46
C	0.19	0.25
D	9.80	9.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.41	1.27
A	1.52	1.72
α	0°	8°
ZD	0.51 REF	
A2	1.37	1.57

SYMBOL	SOIC-16LD INCHES	
	MIN	MAX
A1	.0040	.0098
B	.014	.018
C	.0075	.0098
D	.386	.393
E	.150	.157
e	.050 BSC	
H	.2284	.2440
h	.0099	.0196
L	.016	.050
A	.060	.068
α	0°	8°
ZD	.020 REF	
A2	.054	.062

NOTES :

1. LEAD COPLANARITY SHOULD BE 0 TO 0.10MM (.004") MAX.
2. PACKAGE SURFACE FINISHING :
   (2.1) TOP : MATTE (CHARMILLES #18~30).
3. ALL DIMENSIONS EXCLUDING MOLD FLASHES AND END FLASH FROM THE PACKAGE BODY SHALL NOT EXCEED 0.25MM (.010") PER SIDE(D).

⚠ DETAIL OF PIN #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

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