

Quad LVDS Line Receiver with Extended Common Mode

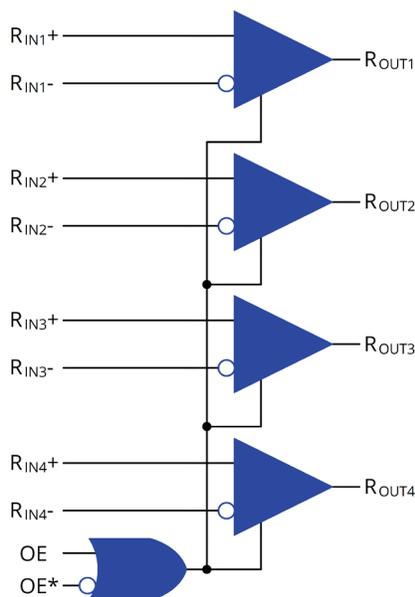
Features

- Extended input common mode voltage range: -7 V to 12 V
- DC to 400 Mbps / 200 MHz low noise, low skew, low power operation
 - 400 ps (max) channel-to-channel skew
 - 300 ps (max) pulse skew
 - 7 mA (max) power supply current
- Open or undriven fail-safe support
- LVDS inputs conform to TIA/EIA-644-A standard
- Standard output enable scheme eliminates power consumption when device is not in use
- Latch-up immune due to dielectric isolation
- Available in space saving SOIC-16 package
- Extended temperature range: -40 °C to +85 °C

Applications

- Data Communications
- Satellite Systems
- Launch Vehicles

Function Diagram



Description

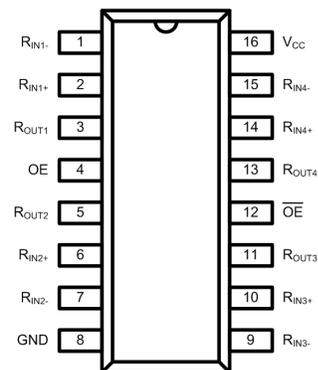
The LVDS032 is a 400 Mbps Quad LVDS (low voltage differential signaling) Line Receiver optimized for high-speed, low power, low noise transmission over controlled impedance (approximately 100 Ω) transmission media (e.g. cables, printed circuit board traces, backplanes).

The LVDS032 accepts four LVDS signals and translates them to four LVCMOS signals. The outputs can be disabled and put in a high-impedance state via two enable pins, OE and OE*.

The LVDS032 input receivers support wide input voltage range of -7 V to 12 V. A fail-safe feature sets the outputs to a high state when the inputs are open, or undriven.

Supply current is 7 mA (max). LVDS outputs conform to the ANSI/EIA/TIA-644-A standard. The LVDS032 is offered in 16-pin SOIC package and operates over an extended -40 °C to +85 °C temperature range.

Pin Diagram



Logic Table

OE	OE*	R _{IN+} - R _{IN-}	R _{OUT}
Any other combination		≥ 100 mV	H
		≤ -100 mV	L
		Fail-safe condition	H
0	1	Don't Care	Disabled

Pin Descriptions

PIN NAME	PIN NUMBER	PIN DESCRIPTION
R_{IN1+} , R_{IN1-} R_{IN2+} , R_{IN2-} R_{IN3+} , R_{IN3-} R_{IN4+} , R_{IN4-}	2, 1, 6, 5, 10, 9, 14, 15	Non-inverting and inverting LVDS receiver input pins.
R_{OUT1} R_{OUT2} R_{OUT3} R_{OUT4}	3, 5, 11, 13	Receiver LVCMOS output pins.
OE, OE*	4, 12	Receiver output enable pins. When OE is high or OE* is low or open, the receiver outputs are enabled. When OE is low and OE* is high, the receiver outputs are disabled.
V_{CC}	16	Power supply pin. Bypass V_{CC} to GND with 0.1 μ F and 0.01 μ F ceramic capacitors.
GND	8	Ground or circuit common pin.

Absolute Maximum Ratings *(NOTE1)*

V_{CC} to GND -0.3 V to +4 V

Inputs

OE, OE* to GND -0.3 V to $V_{CC} + 0.3$ V

R_{IN+} , R_{IN-} to GND -8.0 V to +13.0 V

V_{ID} (R_{IN+} to R_{IN-}) -6.0 V to +6.0 V

Outputs

R_{OUT} to GND -0.3 V to $V_{CC} + 0.3$ V

SOIC-16 Thermal Resistance

Θ_{JC} 41 K/W

Θ_{JA} 72 K/W

T_{stg} - Storage temperature range -65 °C to +150 °C

T_J - Junction operating temperature +150 °C

T_L - Lead temperature (soldering, 4 s) +260 °C

ESD Ratings

HBM *(NOTE2)* 8 kV

MM *(NOTE2)* 250 V

NOTE1 Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE2

HBM - Human Body Model, applicable standard JESD22-A114-C

MM - Machine Model, applicable standard JESD22-A 115-A

Recommended Operating Conditions

Symbol	Parameter	Pins	MIN	TYP	MAX	Unit
V_{CC}	Supply voltage	V_{CC}	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	OE, OE*	2.0		V_{CC}	V
V_{IL}	Low-level input voltage	OE, OE*	0		0.8	V
V_{ID}	Differential input voltage	R_{IN+} , R_{IN-}	0.1	0.35	1.0	V
V_{IN}	Input voltage	R_{IN+} , R_{IN-}	-7		12	V
T_A	Operating free-air temperature range		-40	25	85	°C

Electrical Characteristics

Over recommended operating conditions *(NOTE3)*, $T_A = 25$ °C, $V_{CC} = 3.3$ V, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
LVCMOS Input Specifications (OE, OE* pins)						
V_{IH}	High-level input voltage		2.0		V_{CC}	V
V_{IL}	Low-level input voltage		GND		0.8	V
I_{IH}	High-level input current	$V_{CC} = 3.6$ V, $V_{IN} = 3.6$ V	-10		10	μA
I_{IL}	Low-level input current	$V_{CC} = 3.6$ V, $V_{IN} = 0$ V	-10		10	μA
V_{CL}	Input clamp voltage <i>(NOTE4)</i>	$I_{CL} = -18$ mA, $V_{CC} = 0$ V	-1.5	-0.9		V

Electrical Characteristics (CONTINUED)

Over recommended operating conditions (NOTE3), $T_A = 25\text{ }^\circ\text{C}$, $V_{CC} = 3.3\text{ V}$, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
LVCMOS Output Specifications (R_{OUT} pins)						
V_{OH}	Output high voltage	$I_{OH} = -0.4\text{ mA}$, $V_{ID} = 200\text{ mV}$	2.7	3.2		V
		$I_{OH} = -0.4\text{ mA}$, input open	2.7	3.2		V
V_{OL}	Output low voltage	$I_{OL} = 2.0\text{ mA}$, $V_{ID} = -200\text{ mV}$		0.05	0.25	V
I_{OS}	Output short circuit current (NOTES 3, 5)	Enabled, $V_{OUT} = 0\text{ V}$		-50	-100	mA
I_{OZ}	Output High-Z current	Disabled, $V_{OUT} = 0\text{ V}$ or V_{CC}	-10		10	μA
LVDS Input Specifications (R_{IN+}, R_{IN-} pins)						
V_{TH}	Differential input high threshold	$V_{ICM} = -7\text{ V}$ to 12 V (NOTE6)		0	100	mV
V_{TL}	Differential input low threshold		-100	0		mV
V_{ID}	Differential input voltage		0.1	0.35	1.0	V
V_{ICM}	Input common mode voltage	$V_{ID} = 100\text{ mV}$	-7.0		12.0	V
I_{IN}	Input current $V_{CC} = 0$ or 3.6 V	$0\text{ V} \leq V_{IN+} \leq 2.4\text{ V}$, $V_{IN-} = 1.2\text{ V}$	-15		10	μA
		$-4\text{ V} \leq V_{IN+} \leq 6.4\text{ V}$, $V_{IN-} = \text{open}$	-50		50	μA
		$-7\text{ V} \leq V_{IN+} \leq 12\text{ V}$, $V_{IN-} = \text{open}$	-85		130	μA
C_{IN}	Input capacitance	R_{IN+} or R_{IN-} to GND		4		pF
Power Supply Current Specifications						
I_{CC}	Power supply current	Enabled, not switching		5	7	mA
I_{CCZ}	Power supply current with disabled outputs	Disabled, $OE = 0$ and $OE^* = 1$		1	2	mA

NOTE3 Current into device pin is defined as positive. Current out of the device is defined as negative. All voltages are referenced to ground, unless otherwise specified.

NOTE4 This specification is not production tested and is guaranteed by design simulations.

NOTE5 Output short circuit current (I_{OS}) is specified as magnitude only. The minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification. Specified for momentary short condition durations only.

NOTE6 Recommended operating conditions for the R_{IN+} and R_{IN-} pins is over the range of -7.0 V to 12.0 V . Therefore, caution should be taken not to exceed these values or the maximum Differential input voltage of 1.0 V .

Switching Characteristics

Over recommended operating conditions (**NOTE3**), $T_A = 25\text{ }^\circ\text{C}$, $V_{CC} = 3.3\text{ V}$, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
LVDS AC Specifications (NOTES 7, 8, 9)						
t_{PLH}	Propagation delay, low-to-high	$C_L = 15\text{ pF}$ $V_{ID} = 200\text{ mV}$ $V_{ICM} = 1.2\text{ V}$ (NOTE14) Figures 1 and 2	1.3	2.1	3.3	ns
t_{PHL}	Propagation delay, high-to-low		1.3	2.1	3.3	ns
t_r	Rise time		0.35	1	ns	
t_f	Fall time		0.3	1	ns	
$t_{SK(p)}$	Pulse skew (NOTE10)		50	300	ps	
$t_{SK(c-c)}$	Channel-to-channel skew (NOTE11)		50	400	ps	
$t_{SK(p-p)}$	Part-to-part skew (NOTE12)			1.5	ns	
t_{PLZ}	Disable time, low-to-high Z	$R_L = 2\text{ k}\Omega$ $C_L = 15\text{ pF}$ $V_{ID} = 200\text{ mV}$ $V_{ICM} = 1.2\text{ V}$ (NOTE14) Figures 3 and 4		8	14	ns
t_{PHZ}	Disable time, high-to-high Z			8	14	ns
t_{PZL}	Enable time, high Z-to-low			8	14	ns
t_{PZH}	Enable time, high Z-to-high			8	14	ns
f_{MAX}	Maximum operating frequency (NOTES 13, 14)	$C_L = 15\text{ pF}$ Figure 1		200		MHz

NOTE7 Generator output characteristics (unless otherwise specified): $f = 1\text{ MHz}$, $Z_0 = 50\text{ }\Omega$, $t_r < 1\text{ ns}$, $t_f < 1\text{ ns}$

NOTE8 All Input voltages are for one channel unless otherwise specified. Other inputs are set to GND.

NOTE9 Switching Characteristic specification are not production tested and are guaranteed by statistical analysis of characterization data.

NOTE10 $t_{SK(p)}$ pulse skew, is the magnitude difference in propagation delay time between the positive going edge and the negative going edge of the same channel ($t_{SK(p)} = |t_{PLH} - t_{PHL}|$).

NOTE11 $t_{SK(c-c)}$ channel-to-channel skew, is the difference in propagation delay time between channels on the same device at any operating temperature and supply voltage.

NOTE12 $t_{SK(p-p)}$ part-to-part skew, is the difference in propagation delay time between devices operating at the same power supply voltage and within $5\text{ }^\circ\text{C}$ of each other within the operating temperature range.

NOTE13 Generator output characteristics for the f_{MAX} : $Z_0 = 50\text{ }\Omega$, $t_r = t_f < 1\text{ ns}$, 50 % duty cycle, 1.050 V to 1.35 V peak to peak. Output criteria: 60 % / 40 % duty cycle, V_{OL} (max 0.4 V), V_{OH} (min 2.7 V).

NOTE14 The capacitive load C_L includes test fixture, probe and lumped capacitance.

Test Circuits and Timing Diagrams

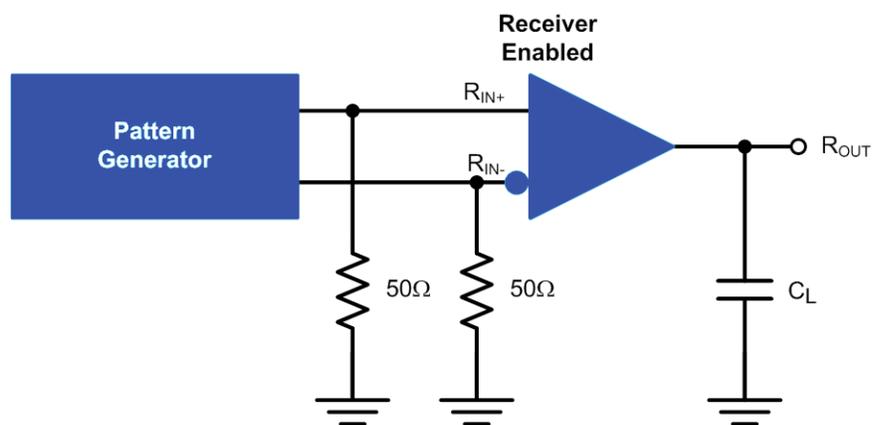


Figure 1. Receiver Propagation Delay and Transition Time Test Setup

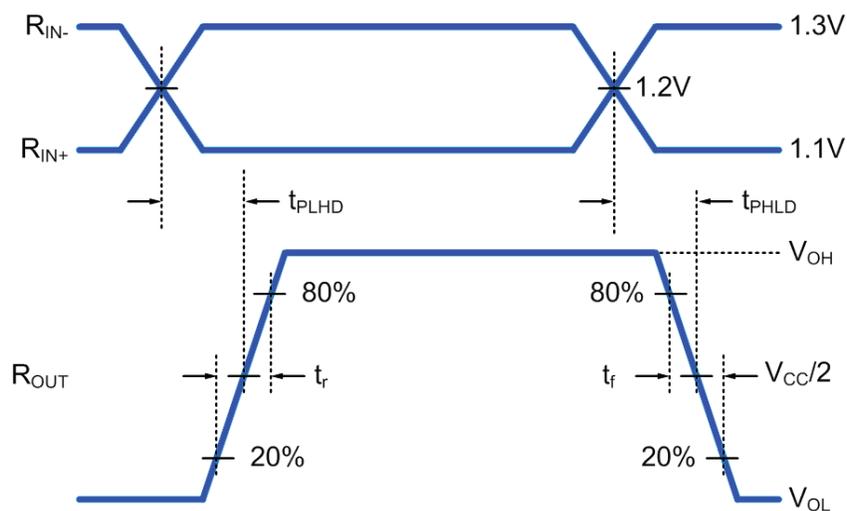


Figure 2. Receiver Propagation Delay and Transition Time Waveforms

Test Circuits and Timing Diagrams

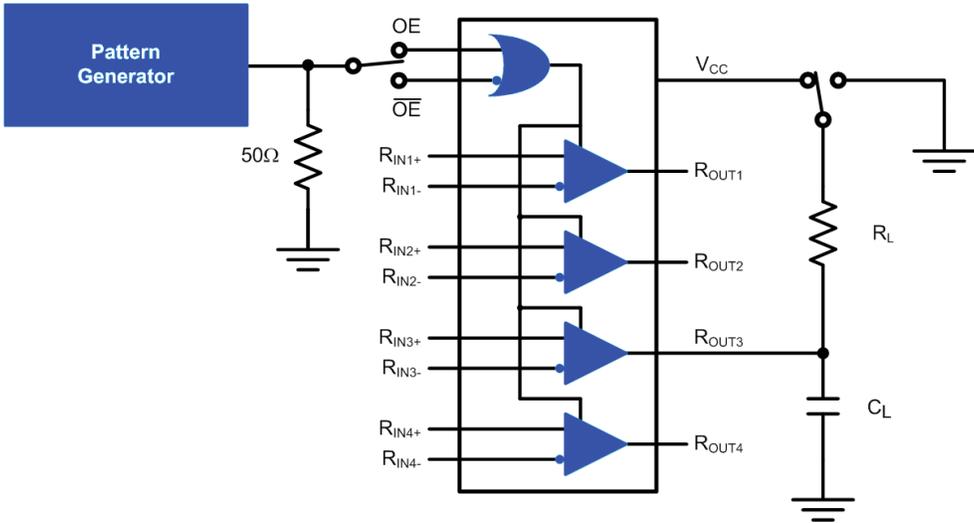


Figure 3. Receiver High-Z Delay Test Setup

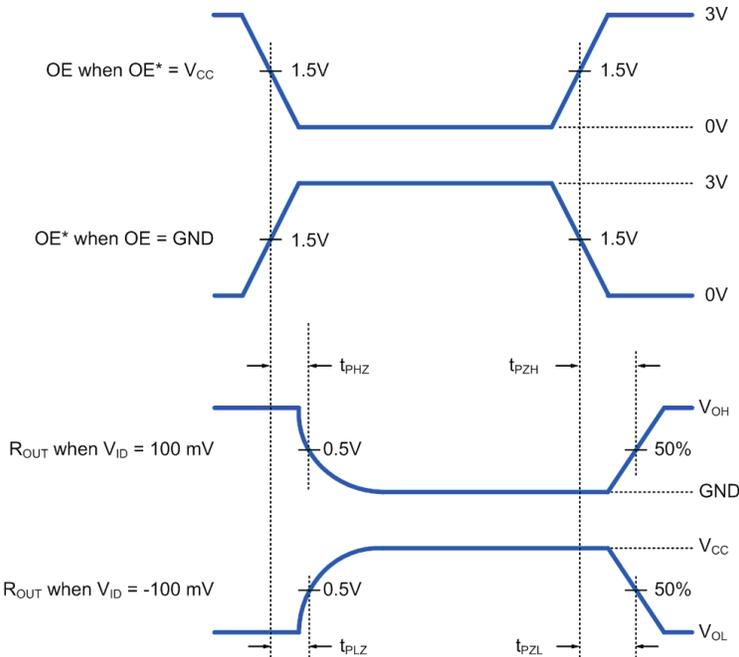


Figure 4. Receiver High-Z Delay Waveforms

Application Information

ABOUT LVDS

Due to bandwidth and power consumption, high speed communication links usually use differential signaling. In this area LVDS provides an outstanding performance to power ratio: It offers a high bandwidth at very low power consumption and low EMI. Therefore it is used extensively for audio and video transmission, ASIC and FPGA I/O, sensor data transmission, clock distribution and a lot more signaling tasks.

COMMON MODE

Large switching currents in an electrical system may result in a momentary voltage drop in supply voltage and/or in a local raise of the ground potential. In terms of the instantaneous ground potential shift this behaviour is known as ground bounce.

This reaction to high currents may be reduced by proper design and size of ground and supply planes and the use of low resistive decoupling capacitors, but they cannot be eliminated totally.

Another effect in this context is a steady-state potential difference between ground connections: Each connection generates a voltage drop which follows Ohm's Law ($U = R * I$). As a result the ground potential difference between a module and the main ground plane rises linearly with current and terminal resistance. Since the terminal resistance may increase by aging, the ground potential of the connected module may drift more and more resulting in a higher steady-state potential difference.

In both situations, ground bounce and ground drift, the common mode difference between transmitter and receiver may exceed the specified ± 1 Volt defined by the LVDS standard resulting in communication errors or even link interruption. These effects have already been reported in Avionics, Industrial applications, by telecommunication companies and automobile manufacturers.

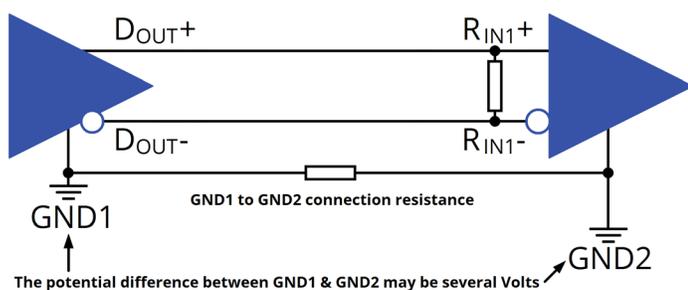


Figure 6. GND-potential difference

POSSIBLE SOLUTION: AC COUPLING?

One possibility to eliminate common mode differences caused by ground potential issues is the use of coupling capacitors on both channels of the differential pair. But there is a big constraint: Capacitive coupling is only convenient for DC balanced data. This means that the data has to have an equal number of ones and zeros. But generally this is not the case for non-coded data, audio, video, sensor or control signals. And if the data would be coded in order to get a balanced signal, this would have an impact on the bandwidth. In case of 8b/10b coding the net data rate will decrease by 20 %.

RS-485

In noisy environments and applications with known common mode issues usually the RS-485/422 is used due to its large swing differential standard which guarantees communication at common modes of -7 to +12 Volts. Its disadvantages are the low data rate and the poor bandwidth to power and EMI performance.

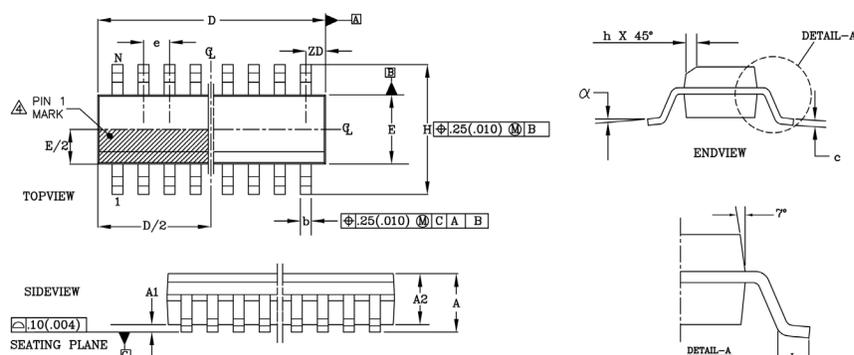
EXTENDED COMMON-MODE LVDS: COMBINING THE ADVANTAGES

Having a look at the LVDS standard, the noise margin may be sufficient on single PCBs or in small boxed systems. But in noisy environments or larger distributed systems or box-to-box communication, the small ± 1 V common mode window potentially leads to communication problems, particularly over the lifetime of the system.

RS-485 offers a much better noise margin but shows very poor performance regarding power consumption, speed and EMI.

Extended common-mode LVDS combines the benefits of LVDS and RS-485: It's fully compatible with the LVDS standard in terms of signal levels, speed, power and EMI, showing the standard pinout and footprint. The extended common mode of -7 to +12 Volt finally makes it a perfect choice for harsh environments. Also it works as a high-performance replacement for RS-485 applications.

Package Dimensions (SOIC-16)



SOIC-16LD		
SYMBOL	MILLIMETERS	
	MIN	MAX
A1	0.10	0.25
B	0.36	0.46
C	0.19	0.25
D	9.80	9.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.41	1.27
A	1.52	1.72
α	0°	8°
ZD	0.51	REF
A2	1.37	1.57

SOIC-16LD		
SYMBOL	INCHES	
	MIN	MAX
A1	.0040	.0098
B	.014	.018
C	.0075	.0098
D	.386	.393
E	.150	.157
e	.050 BSC	
H	.2284	.2440
h	.0099	.0196
L	.016	.050
A	.060	.068
α	0°	8°
ZD	.020	REF
A2	.054	.062

NOTES :

- LEAD COPLANARITY SHOULD BE 0 TO 0.10MM (.004") MAX.
- PACKAGE SURFACE FINISHING :
(2.1) TDP : MATTE (CHARMILLES #18-30).
- ALL DIMENSIONS EXCLUDING MOLD FLASHES AND END FLASH FROM THE PACKAGE BODY SHALL NOT EXCEED 0.25MM (.010") PER SIDE(D).

▲ DETAIL OF PIN #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

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